

## 4-Mbit (256K x 16) Static RAM

### Features

- Very high speed: 45 ns
- Wide voltage range: 2.20V–3.60V
- Pin compatible with CY62146DV30
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 7  $\mu$ A
- Ultra low active power
  - Typical active current: 2 mA @ f = 1 MHz
- Easy memory expansion with  $\overline{CE}$ , and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in a Pb-free 48-ball VFBGA and 44-pin TSOP II packages

### Functional Description <sup>[1]</sup>

The CY62146EV30 is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly

reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH). The input and output pins (IO<sub>0</sub> through IO<sub>15</sub>) are placed in a high impedance state when:

- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH)
- Write operation is active ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW)

Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from IO pins (IO<sub>0</sub> through IO<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

Read from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on IO<sub>0</sub> to IO<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on IO<sub>8</sub> to IO<sub>15</sub>. See the “Truth Table” on page 9 for a complete description of read and write modes.

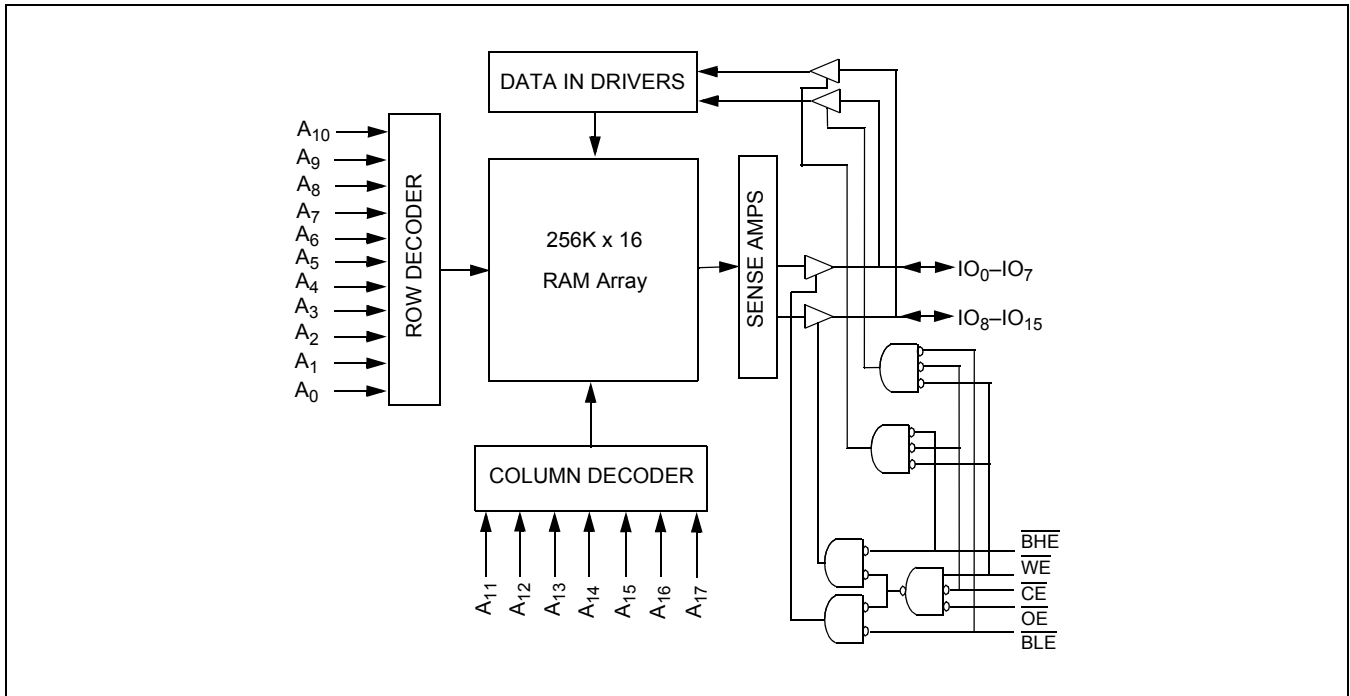
### Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> ( $\mu$ A)	
					f = 1 MHz		f = f <sub>max</sub>			
Min	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max		
CY62146EV30LL	2.2	3.0	3.6	45 ns	2	2.5	15	20	1	7

#### Notes:

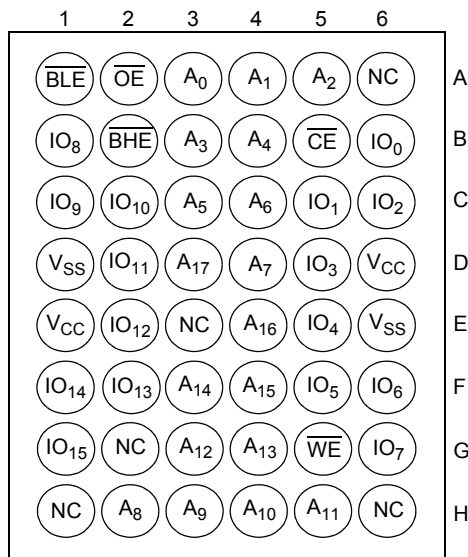
1. For best practice recommendations, please refer to the Cypress application note *System Design Guidelines* on <http://www.cypress.com>.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.

**Logic Block Diagram**

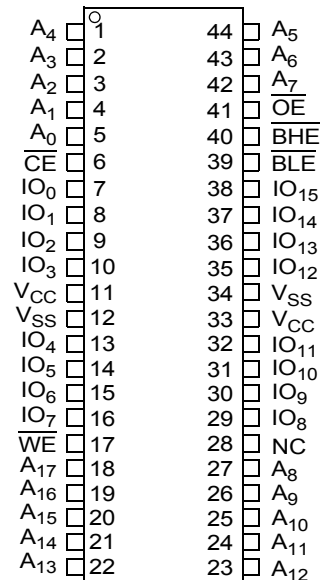


**Pin Configurations [3, 4]**

**48-ball VFBGA  
Top View**



**44-pin TSOP II  
Top View**



**Notes:**

- 3. NC pins are not connected on the die.
- 4. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8 Mb, 16 Mb and 32 Mb, respectively.

### Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to + 150°C

Ambient Temperature with Power Applied ..... -55°C to + 125°C

Supply Voltage to Ground Potential ..... -0.3V to + 3.9V ( $V_{CCmax} + 0.3V$ )

DC Voltage Applied to Outputs in High-Z State <sup>[5, 6]</sup> ..... -0.3V to 3.9V ( $V_{CCmax} + 0.3V$ )

DC Input Voltage <sup>[5, 6]</sup> ..... -0.3V to 3.9V ( $V_{CCmax} + 0.3V$ )

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

### Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[7]</sup>
CY62146EV30	Industrial	-40°C to +85°C	2.2V to 3.6V

### Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ <sup>[2]</sup>	Max	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	2.0			V
		I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> ≥ 2.70V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA			0.4	V
		I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> ≥ 2.70V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.2V to 2.7V	1.8		V <sub>CC</sub> + 0.3	V
		V <sub>CC</sub> = 2.7V to 3.6V	2.2		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.2V to 2.7V	-0.3		0.6	V
		V <sub>CC</sub> = 2.7V to 3.6V	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>max</sub> = 1/t <sub>RC</sub>		15	20	mA
		f = 1 MHz	V <sub>CC</sub> = V <sub>CC(max)</sub> , I <sub>OUT</sub> = 0 mA CMOS levels	2	2.5	
I <sub>SB1</sub>	Automatic CE Power down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V f = f <sub>max</sub> (Address and Data Only), f = 0 ( $\overline{OE}$ , $\overline{BHE}$ , $\overline{BLE}$ and $\overline{WE}$ ), V <sub>CC</sub> = 3.60V		1	7	μA
I <sub>SB2</sub> <sup>[8]</sup>	Automatic CE Power down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.60V		1	7	μA

#### Notes:

- V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
- Only chip enable ( $\overline{CE}$ ) and byte enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) need to be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

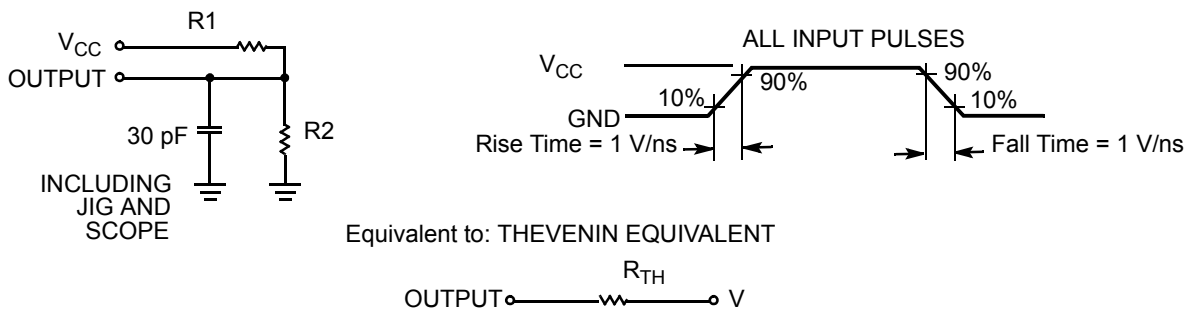
**Capacitance** (For All Packages) <sup>[9]</sup>

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Thermal Resistance** <sup>[9]</sup>

Parameter	Description	Test Conditions	VFBGA Package	TSOP II Package	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	77	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		10	13	°C/W

**AC Test Loads and Waveforms**

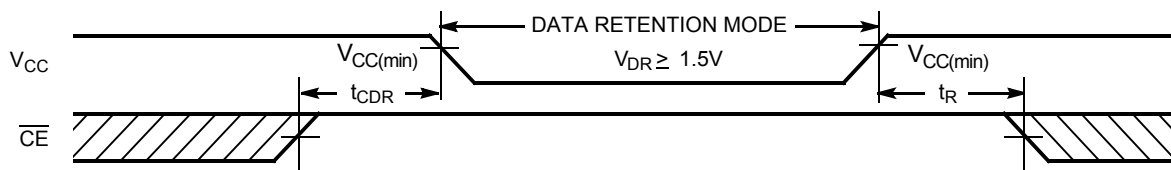


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

**Data Retention Characteristics** (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ <sup>[2]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5			V
I <sub>CCDR</sub> <sup>[8]</sup>	Data Retention Current	V <sub>CC</sub> = 1.5V, $\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		0.8	7	μA
t <sub>CDR</sub> <sup>[9]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[10]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform**



**Notes:**

- 9. Tested initially and after any design or process changes that may affect these parameters.
- 10. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

**Switching Characteristics** (Over the Operating Range) <sup>[11, 12]</sup>

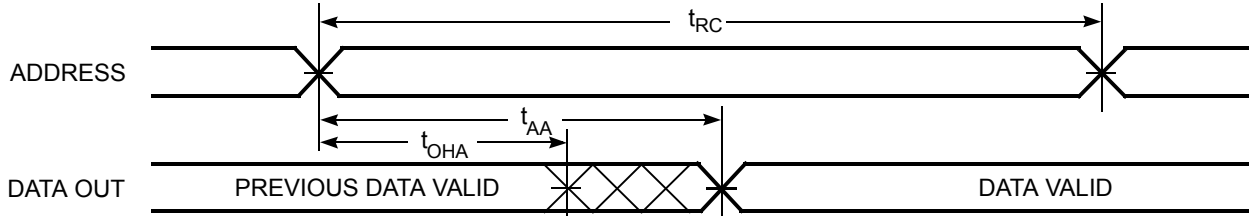
Parameter	Description	45 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read Cycle Time	45		ns
$t_{AA}$	Address to Data Valid		45	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[13]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[13, 14]</sup>		18	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low-Z <sup>[13]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High-Z <sup>[13, 14]</sup>		18	ns
$t_{PU}$	$\overline{CE}$ LOW to Power Up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power Down		45	ns
$t_{DBE}$	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		22	ns
$t_{LZBE}$	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z <sup>[13]</sup>	5		ns
$t_{HZBE}$	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z <sup>[13, 14]</sup>		18	ns
<b>Write Cycle</b> <sup>[15]</sup>				
$t_{WC}$	Write Cycle Time	45		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	35		ns
$t_{AW}$	Address Setup to Write End	35		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Setup to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35		ns
$t_{BW}$	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	35		ns
$t_{SD}$	Data Setup to Write End	25		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[13, 14]</sup>		18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[13]</sup>	10		ns

**Notes:**

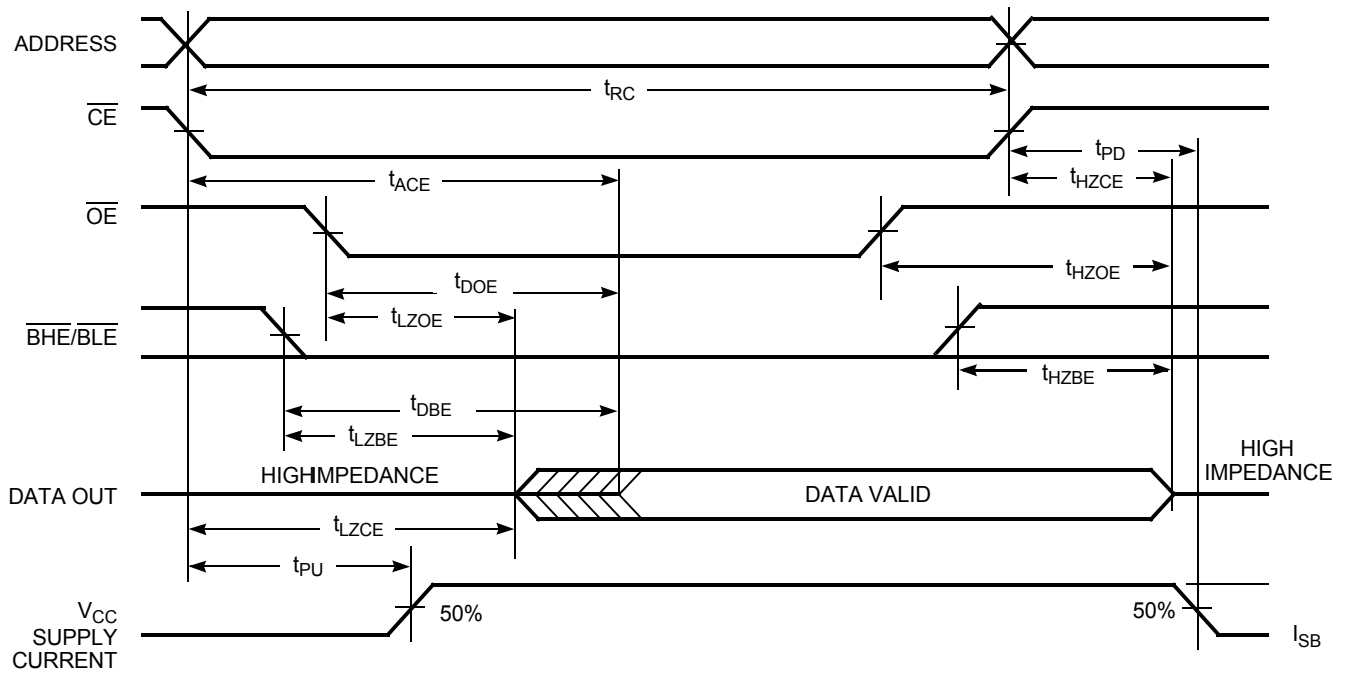
- Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" on page 4.
- AC timing parameters are subject to byte enable signals ( $\overline{BHE}$  or  $\overline{BLE}$ ) not switching when chip is disabled. Please see application note AN13842 for further clarification.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

Read Cycle 1 (Address Transition Controlled) [16, 17]



Read Cycle No. 2 ( $\overline{OE}$  Controlled) [17, 18]

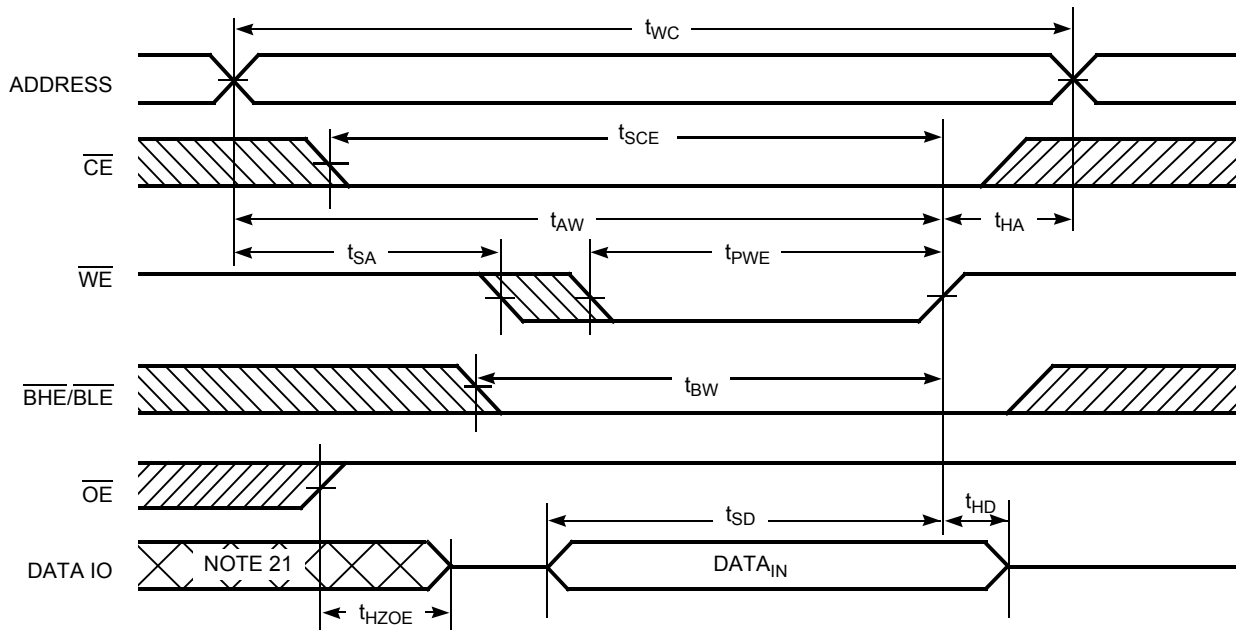


**Notes:**

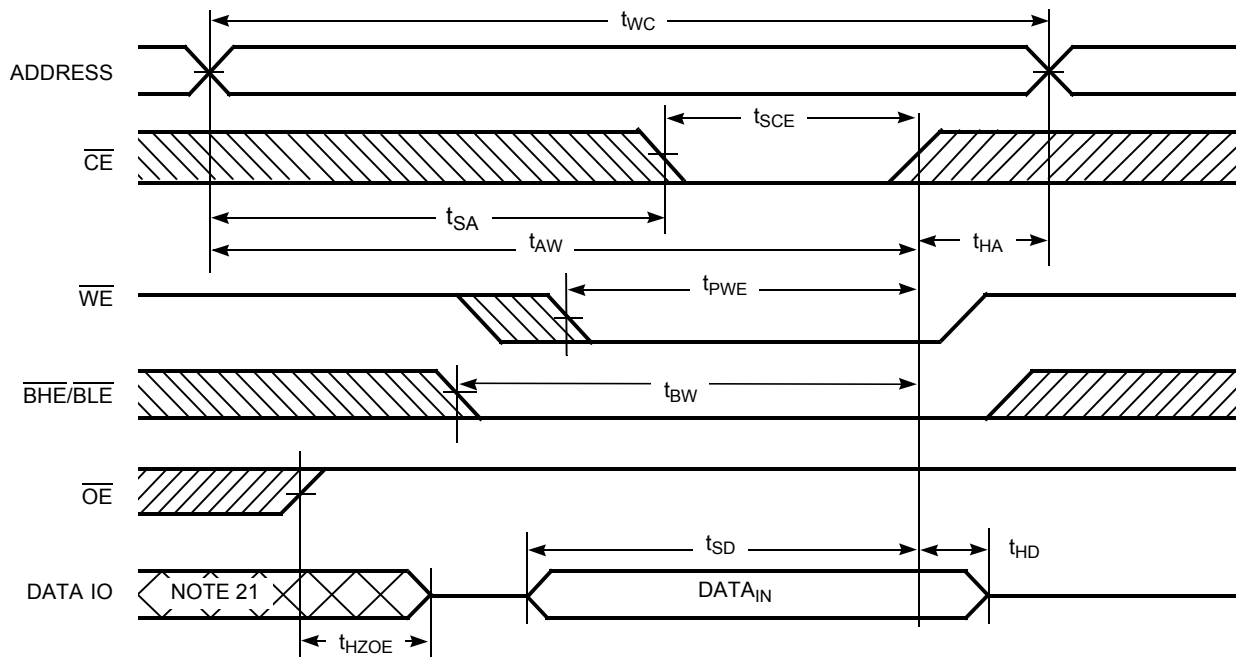
- 16. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
- 17.  $\overline{WE}$  is HIGH for read cycle.
- 18. Address valid before or similar to  $\overline{CE}$  and  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

**Switching Waveforms (continued)**

**Write Cycle No. 1 ( $\overline{WE}$  Controlled) [15, 19, 20]**



**Write Cycle No. 2 ( $\overline{CE}$  Controlled) [15, 19, 20]**

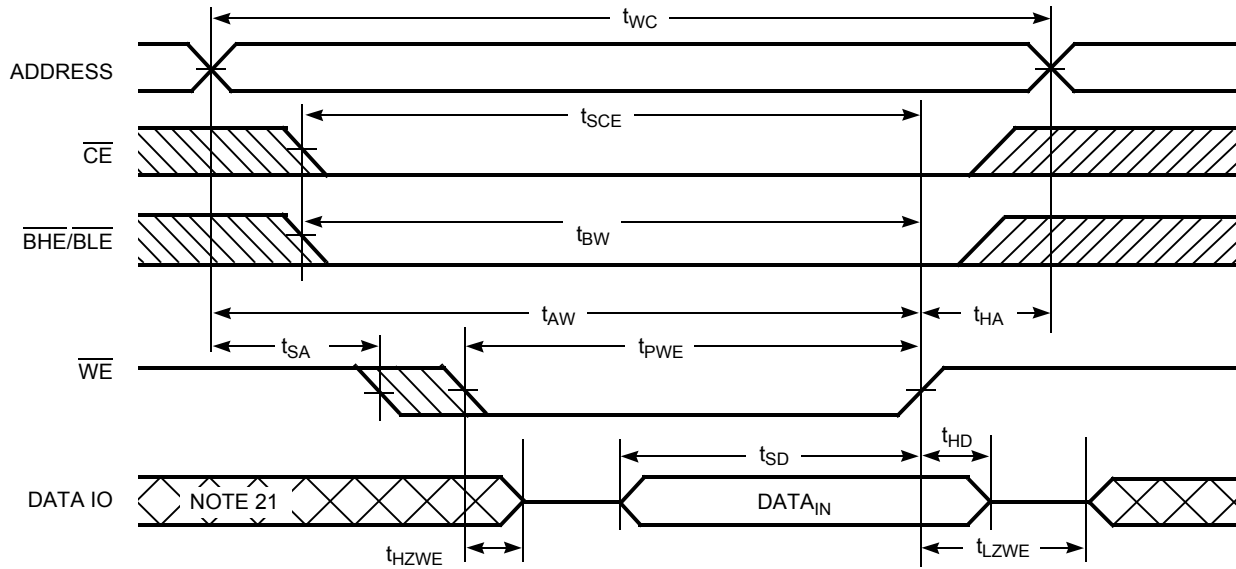


**Notes:**

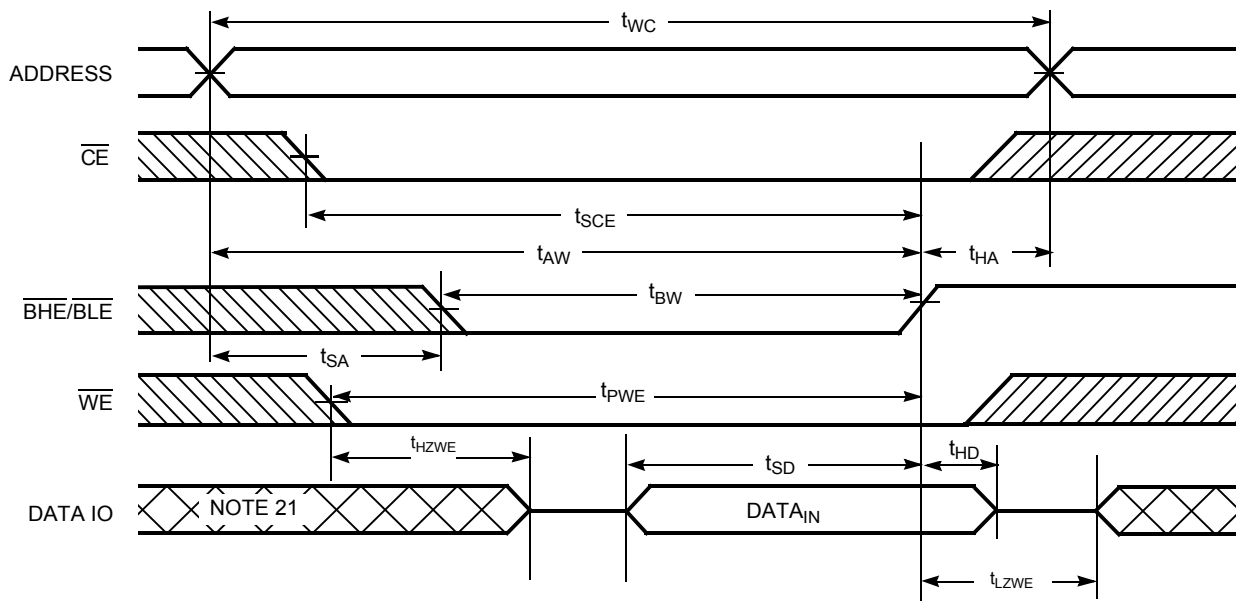
- 19. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
- 20. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 21. During this period, the IOs are in output state and input signals must not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [20]



Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW) [20]





**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power down	Standby ( $I_{\text{SB}}$ )
L	X	X	H	H	High-Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	L	L	L	Data Out ( $\text{IO}_0\text{--}\text{IO}_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	L	H	L	Data Out ( $\text{IO}_0\text{--}\text{IO}_7$ ); $\text{IO}_8\text{--}\text{IO}_{15}$ in High-Z	Read	Active ( $I_{\text{CC}}$ )
L	H	L	L	H	Data Out ( $\text{IO}_8\text{--}\text{IO}_{15}$ ); $\text{IO}_0\text{--}\text{IO}_7$ in High-Z	Read	Active ( $I_{\text{CC}}$ )
L	H	H	L	L	High-Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	H	H	L	High-Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	H	L	H	High-Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	L	X	L	L	Data In ( $\text{IO}_0\text{--}\text{IO}_{15}$ )	Write	Active ( $I_{\text{CC}}$ )
L	L	X	H	L	Data In ( $\text{IO}_0\text{--}\text{IO}_7$ ); $\text{IO}_8\text{--}\text{IO}_{15}$ in High-Z	Write	Active ( $I_{\text{CC}}$ )
L	L	X	L	H	Data In ( $\text{IO}_8\text{--}\text{IO}_{15}$ ); $\text{IO}_0\text{--}\text{IO}_7$ in High-Z	Write	Active ( $I_{\text{CC}}$ )

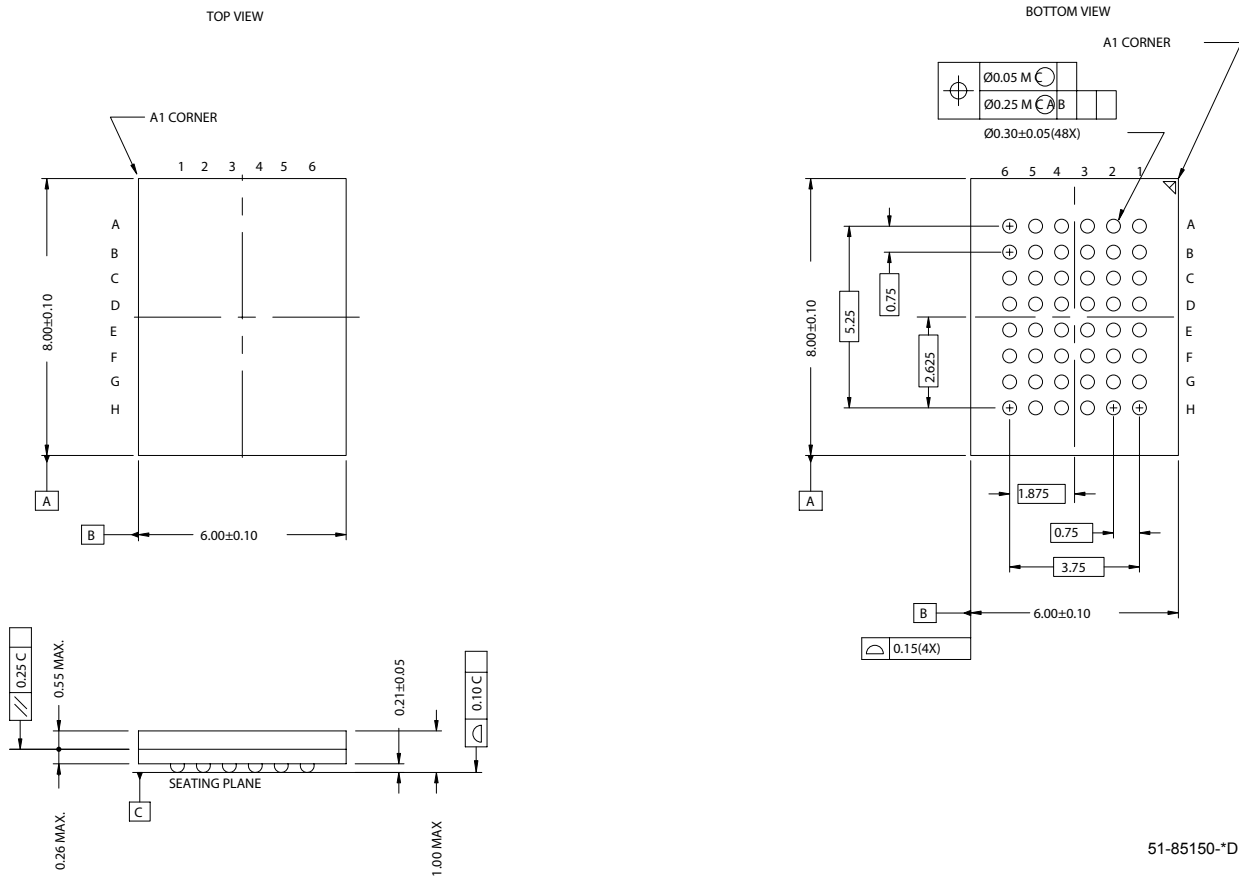
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62146EV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Please contact your local Cypress sales representative for availability of other parts

Package Diagrams

Figure 1. 48-ball VFBGA (6 x 8 x 1 mm), 51-85150

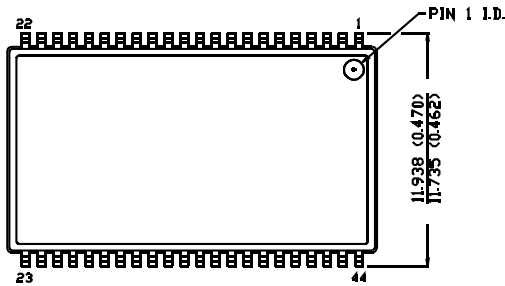


51-85150-\*D

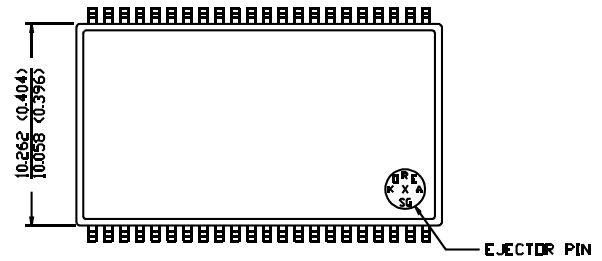
Package Diagrams (continued)

Figure 2. 44-pin TSOP II, 51-85087

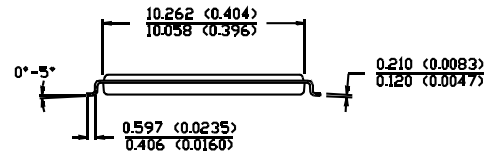
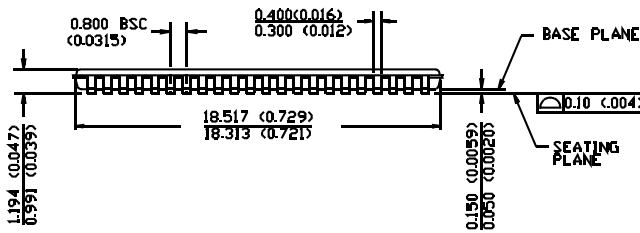
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



BOTTOM VIEW



51-85087-\*A

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**Document History Page**

Document Title: CY62146EV30 MoBL®, 4-Mbit (256K x 16) Static RAM				
Document Number: 38-05567				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	223225	See ECN	AJU	New Data Sheet
*A	247373	See ECN	SYT	<p>Changed Advance Information to Preliminary</p> <p>Moved Product Portfolio to Page 2</p> <p>Changed <math>V_{CC}</math> stabilization time in footnote #8 from 100 <math>\mu</math>s to 200 <math>\mu</math>s</p> <p>Removed Footnote #14(<math>t_{LZBE}</math>) from Previous revision</p> <p>Changed <math>I_{CCDR}</math> from 2.0 <math>\mu</math>A to 2.5 <math>\mu</math>A</p> <p>Changed typo in Data Retention Characteristics(<math>t_R</math>) from 100 <math>\mu</math>s to <math>t_{RC}</math> ns</p> <p>Changed <math>t_{OHA}</math> from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin</p> <p>Changed <math>t_{HZOE}</math>, <math>t_{HZBE}</math>, <math>t_{HZWE}</math> from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin</p> <p>Changed <math>t_{SCE}</math> and <math>t_{BW}</math> from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin</p> <p>Changed <math>t_{HZCE}</math> from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin</p> <p>Changed <math>t_{SD}</math> from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin</p> <p>Changed <math>t_{DOE}</math> from 15 to 18 ns for 35 ns Speed Bin</p> <p>Changed <math>t_{DBE}</math> from 15 to 18 ns for 35 ns Speed Bin</p> <p>Changed Ordering Information to include Pb-Free Packages</p>
*B	414807	See ECN	ZSD	<p>Changed from Preliminary information to Final</p> <p>Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed 35ns Speed Bin</p> <p>Removed "L" version of CY62146EV30</p> <p>Changed ball E3 from DNU to NC</p> <p>Removed the redundant foot note on DNU.</p> <p>Changed <math>I_{CC}</math> (Max) value from 2 mA to 2.5 mA and <math>I_{CC}</math> (Typ) value from 1.5 mA to 2 mA at <math>f=1</math> MHz</p> <p>Changed <math>I_{CC}</math> (Typ) value from 12 mA to 15 mA at <math>f = f_{max}</math></p> <p>Changed <math>I_{SB1}</math> and <math>I_{SB2}</math> Typ values from 0.7 <math>\mu</math>A to 1 <math>\mu</math>A and Max values from 2.5 <math>\mu</math>A to 7 <math>\mu</math>A.</p> <p>Changed the AC test load capacitance from 50pF to 30pF on Page# 4</p> <p>Changed <math>I_{CCDR}</math> from 2.5 <math>\mu</math>A to 7 <math>\mu</math>A.</p> <p>Added <math>I_{CCDR}</math> typical value.</p> <p>Changed <math>t_{LZOE}</math> from 3 ns to 5 ns</p> <p>Changed <math>t_{LZCE}</math> and <math>t_{LZWE}</math> from 6 ns to 10 ns</p> <p>Changed <math>t_{LZBE}</math> from 6 ns to 5 ns</p> <p>Changed <math>t_{HZCE}</math> from 22 ns to 18 ns</p> <p>Changed <math>t_{PWE}</math> from 30 ns to 35 ns.</p> <p>Changed <math>t_{SD}</math> from 22 ns to 25 ns.</p> <p>Updated the package diagram 48-ball VFBGA from *B to *D</p> <p>Updated the ordering information table and replaced the Package Name column with Package Diagram.</p>
*C	925501	See ECN	VKN	<p>Added footnote #8 related to <math>I_{SB2}</math> and <math>I_{CCDR}</math></p> <p>Added footnote #12 related AC timing parameters</p>